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Effects of $LaNiO_3$ bottom electrode on structural and dielectric properties of $CaCu_3Ti_4O_{12}$ films fabricated by sol-gel method

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$CaCu_3Ti_4O_{12}$ (CCTO) thin films are prepared by a sol-gel method on $LaNiO_3$-coated silicon and $Pt/TiO_2/SiO_2/Si$ substrate. Compared with the films on Pt, the CCTO on $LaNiO_3$ exhibits a (400) orientation. Dielectric loss of CCTO on $LaNiO_3$ is lower than 0.25 within 100 Hz–10 kHz, lower than the reported value of CCTO grown on $Pt/TiO_2/SiO_2/Si$ by pulse laser deposition. Possible reason is that $LaNiO_3$ acts as seed layer for the growth of CCTO. The crystallinity of CCTO is improved and the dielectric properties are enhanced. Complex impedance spectrum of CCTO on $LaNiO_3$ is discussed according to grain boundary barrier layer capacitance model. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2837534]

In recent years, the compound $CaCu_3Ti_4O_{12}$ (CCTO) has attracted considerable attention because of its special dielectric properties.[1–10] This material in ceramic and single-crystalline forms exhibits a colossal relative permittivity ε' up to 10^4 at room temperature in the frequency range between dc and 10^6 Hz. Furthermore, it was found that the permittivity is independent of temperature between 100 and 380 K.[1–3] All of these special properties promote the potential applications of this material in the field of microelectronic devices, such as static and dynamic random access memories.[2] At the same time, studies on the origin of the unusual dielectric behavior have also been carried out. Subramanian *et al.*,[1] Homes *et al.*,[2] and Ramirez *et al.*[4] attributed the origin of the high permittivity to the intrinsic crystal structure of CCTO. Cohen *et al.*,[6] Lunkenheimer *et al.*,[7] Chiodeli *et al.*,[8] and Zhang and Tang[9] suggested that the special dielectric behaviors came from the extrinsic electrical inhomogeneity of CCTO, for example, the grain boundary barrier layer capacitance (IBLC) model.[8,9]

Compared with single crystal and ceramic, thin film is convenient for application in devices. Up to now, CCTO thin films have been grown on $LaAlO_3$, $SrTiO_3$, and $Pt/TiO_2/SiO_2/Si$ substrates by pulse laser deposition (PLD) method.[10–14] The CCTO thin films grown directly on $LaAlO_3$ and $SrTiO_3$ single crystal substrates exhibit high-quality epitaxial characteristics. However, the films grown on the substrates with metal electrode display higher low-frequency dielectric loss. As reported, the high dielectric loss and large leakage current are the critical problems for the application of CCTO.[15] Some groups fabricate CCTO thin films by chemical solution route or sol-gel method but there are no data about the dielectric measurements in their works.[16,17] One of the possible reasons is that the high dielectric loss disturbed their measurement. Therefore, the decrease of low-frequency dielectric loss is significant for the application of CCTO. Fang *et al.* reported the decrease of the dielectric loss by introducing $CaTiO_3$ buffer layer between CCTO thin film and Pt electrode.[10] However, this method increases the complexity of the thin film preparation and it is possible to introduce unexpected defects to the sample, such as interface. As a typical conductive oxide, $LaNiO_3$ (LNO) has been used as bottom electrode to improve the structural and electric properties of ferroelectric thin films.[18–20] In this letter, we studied the effect of LNO bottom electrode on the structural and dielectric properties of CCTO thin films fabricated by sol-gel method.

LNO electrodes were fabricated by chemical solution deposition on Si(100) substrate. Details about the preparation of $LaNiO_3$ thin films have been reported.[18] CCTO thin films were derived by sol-gel method. Calcium nitrate, copper nitrate, and titanium isopropoxide were used as stuff to prepare the CCTO precursor. The CCTO thin films were deposited by spin coating the precursor to substrate and then annealing in a rapid thermal process (RTP) furnace. The spin coating and annealing process were repeated several times before the thin films archived expected thickness of 180 nm. For convenience to observe the effect of LNO bottom electrode, the CCTO thin films were also prepared on $Pt/TiO_2/SiO_2/Si$ substrate correspondingly. The structure and phase composition of the films were analyzed by x-ray diffraction (XRD). Surface and cross-sectional microstructure of the films were observed by scanning electron microscopy (SEM). For electrical measurements, Pt top electrodes with 0.2 mm diameter were prepared through a shadow mask. Measurements on the dielectric properties of the samples were performed in the frequency range of 100 Hz–100 kHz with an applied voltage of 100 mV using a Hewlett-Packard Impedance Analyzer, model 4194A.

XRD patterns of CCTO thin films grown on LNO-coated Si(100) and $Pt/TiO_2/SiO_2/Si$ are shown in Fig. 1. All the observed peaks are derived from the CCTO thin films and the substrates without any hint of an impurity phase. Compared with the films grown on Pt, the relative intensity of (220) peak for CCTO films grown on LNO decreases markedly, whereas the relative intensity of (400) peak enhances. This means that the CCTO thin films grown on LNO possess (400) preferential orientation compared with the films on Pt.

The surface and cross-sectional SEM images of the films on LNO and Pt are presented in Fig. 2. A large number of pinholes can be observed from the surface SEM images of

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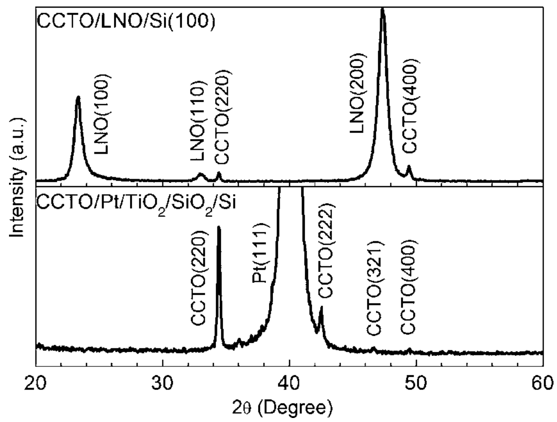

FIG. 1. XRD patterns of CCTO grown on LNO and Pt.

the two samples but the cross-sectional SEM image indicates that the CCTO thin film is more condensed than the LNO layer. The possible reason is the influence from preparation process. When the wet film of CCTO is annealed in RTP furnace, many pinholes are formed at the surface of the CCTO films. When next layer precursor is spin coated on it and annealed, crystal grains fill in the pinhole, therefore, inner of the CCTO thin films is dense. This explanation is also proven by the difference of the CCTO/LNO interface and CCTO/Pt interface. It is obvious that interface between CCTO and Pt is clear but the interface between CCTO and LNO is blurry. It is because LNO provides some positions at its surface, such as pinhole or other defect, as the nucleation site of CCTO. That is why the interface between CCTO and LNO is illegible. Therefore, during the growth of CCTO thin films, the LNO thin films act not only as electrode but also as the seed layer, whereas the compact Pt cannot offer such positions at its surface, the crystal nucleus of CCTO is formed just at the inner of CCTO layer, so the interface between CCTO and Pt is legible.

The dielectric measurements are carried out at room temperature. However, the leakage current of CCTO thin films grown on Pt is too high to detect it. The measurement about the CCTO thin films on LNO is performed. The capacitance and dielectric loss (tan δ) of the CCTO thin films grown on LNO are shown in Fig. 3. The capacitance decreases with the frequency increasing. The dielectric loss shows moderate decrease with the frequency below 1.2 kHz and abrupt increase when the frequency is beyond 10 kHz. The profile of the frequency dependence of dielectric loss is similar to the result of CCTO thin films prepared by PLD.[15] The tan δ is lower than 0.25 within the frequency range of 100 Hz–10 kHz. The value of tan δ at lowest frequency 100 Hz is 0.248. This value is lower than the CCTO thin films grown on Pt by PLD Refs. 10 and 21 and close to the value of CCTO thin films with $CaTiO_3$ buffer layer.[15] The possible reason of the suppressed dielectric loss is the effect from LNO as seed layer. The LNO seed layer improves the crystallinity of CCTO thin films so that the dielectric properties, which are associated with the microstructure and crystallinity of films, are also improved. The seed layer has been used to interpret the effect of $CaTiO_3$ buffer layer on dielectric properties of CCTO thin films.[15] Our result indicates that the electric properties of CCTO thin films can be improved by using LNO substituting metal electrode.

The dielectric properties of CCTO thin films grown on LNO are also analyzed in complex impedance plane. According to IBLC model, the equivalent circuit of CCTO can be expressed as two parallel *RC* elements connected in series, as shown in the inset of Fig. 4, one *RC* element $R_b C_b$ representing the semiconducting grains and the other $R_{gb} C_{gb}$ representing the insulating grain boundary regions.[22,23] The pattern of Z'' (real part of complex impedance Z^*) versus Z' (imaginary part of complex impedance Z^*) in complex impedance plane should be two semicircular arcs intercepting the Z' axis at R_b (higher frequency) and R_{gb} (lower fre-

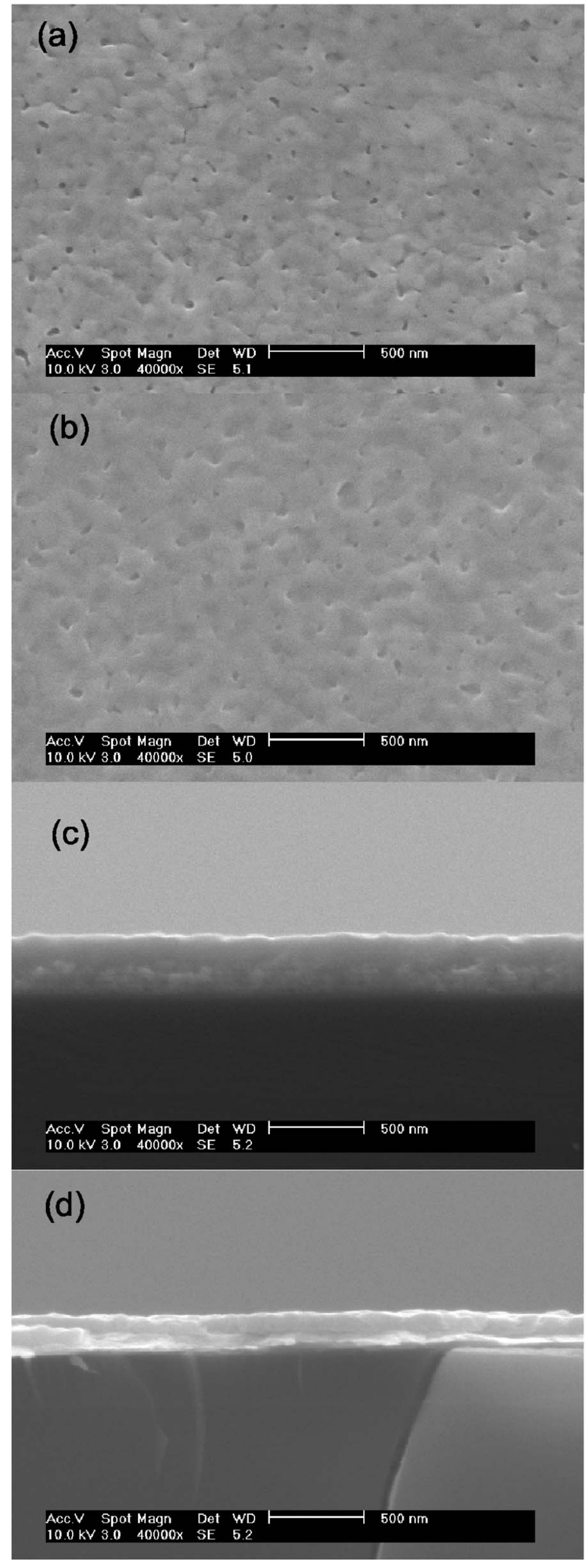

FIG. 2. Surface and cross-sectional SEM images of CCTO thin films grown on [(a) and (c)] LNO and [(b) and (d)] Pt.

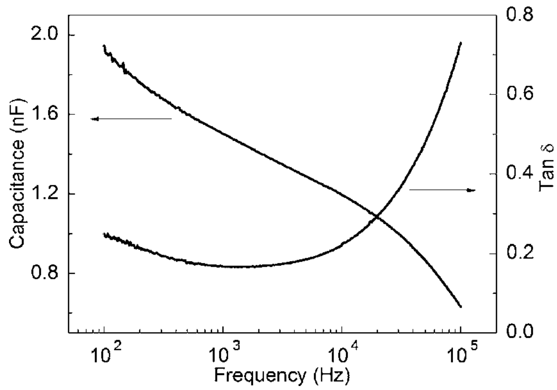

FIG. 3. The frequency dependence of capacitance and dielectric loss of CCTO thin films on LNO.

quency). Z'' achieves maximum when frequency ω equals to the relaxation frequency $\omega_\tau = 1/RC$.[22,23] The complex impedance spectroscopy of the CCTO thin films on LNO is shown in Fig. 4. Because the relax frequency ω_τ is lower than 100 Hz, exceeded the frequency range of the measurement, the exact value of R_{gb} at low frequency cannot be educed from the impedance spectroscopy. Nevertheless, the estimated value of R_{gb} is not less than 300 kΩ. R_b can be inferred by intercepting the high frequency region of the impedance spectroscopy with the Z' axis. The value is about 1 kΩ, as shown in the inset of Fig. 4.

It should been pointed out that the relative permittivity of the CCTO thin films in our experiment is much smaller than bulk material (about 1300 at 100 Hz). Similar behavior has been observed by Si *et al.* in CCTO thin films prepared by PLD.[24] There is no particular explanation in their paper. As for our samples, the possible reason is that the grain size in the present sample is too small. The samples are annealed in a RTP furnace and the time of thermal process is very short. The average grain size is about 80 nm from the SEM image, which is much smaller than that in CCTO ceramics (at the magnitude of micron).[3,25] Based on recent reports, the relative permittivity of CCTO ceramic increases with the grain size increasing.[3,25] Therefore, if the crystal grain in our sample can have a larger size, it is possible to fabricate

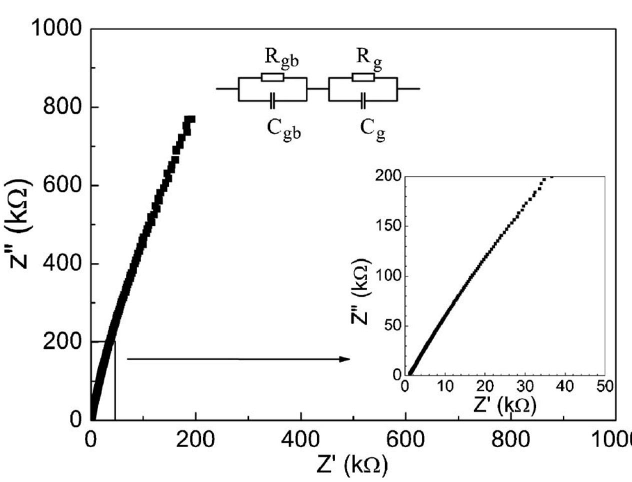

FIG. 4. The complex impedance plane plot for the CCTO thin films grown on LNO. The upper inset shows the equivalent circuit used to represent the electrical properties of grain and grain-boundary effects and the lower inset shows the intercept on Z' axis.

CCTO thin films with giant relative permittivity and low dielectric loss by growing the films on conductive oxide electrode.

In conclusion, the CCTO thin films are fabricated on both LNO-coated silicon substrate and $Pt/TiO_2/SiO_2/Si$ substrate by sol-gel method. Compared with the samples on Pt, the films on LNO possess the (400) preferential orientation. It indicates that the low-frequency dielectric loss of CCTO thin films on LNO is smaller than that grown on metal electrode. The reason is that the $LaNiO_3$ act as seed layer during the crystallization of CCTO thin films and the crystallinity of CCTO thin films is improved. Therefore, the dielectric properties of the CCTO thin films are enhanced. This result is beneficial for the potential application of CCTO thin films in microelectronic devices.

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