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Lattice vibration characteristics in layered InSe films and the electronic behavior of field-effect transistors

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Abstract

Understanding how temperature affects the structural and electronic properties for two-dimensional (2D) semiconductors could promote the application and development of nanoelectronic devices. Here, the temperature dependence of lattice structure for indium selenide (InSe) nanosheets and the corresponding electronic properties of 3 nm indium-deposited InSe field-effect transistors (FETs) are systematically demonstrated. Analyses of Raman spectra suggest that the difference of phonon frequency ($\Delta\omega$) for the A^2_{1g} mode is found to be 3.14 cm^{-1}, which is larger than that of the E^1_{2g} mode due to the stronger electron-phonon coupling for the A^2_{1g} mode. The device performance based on indium-deposited InSe is systematically explained using Kelvin probe force microscopy (KPFM) and the predicted energy band structure. Furthermore, FETs based on temperature and variable thickness InSe flakes are designed as applicable devices. Our findings are of fundamental importance to explain the underlying physics in intrinsic InSe transistors and improve further applications.

Keywords: InSe, lattice vibration, field-effect transistor, temperature dependence

(Some figures may appear in colour only in the online journal)

1. Introduction

The unique structural features and prominent electronic properties of two-dimensional (2D) semiconductors are motivating the development of the next generation of electronic devices to the atomic dimension and with higher integration levels for premium performance. The family of 2D semiconductor is gradually being expanded to include graphene, black phosphorus, transition metal dichalcogenides (TMDs) and others [1–4]. Graphene and black phosphorus show excellent intrinsic charge carrier conduction characteristics [5]. However, some obvious drawbacks, such as the zero-bandgap of graphene and the chemical corruptible properties of black phosphorus in air conditions have hindered their practical applications [5–8]. TMDs usually suffer from a mobility-ceiling of 1000 $cm^2V^{-1}s^{-1}$ which is unexpected in the development of high-speed logic circuits or high-frequency devices [9]. A novel layered indium selenide (InSe) semiconductor, with ultrahigh carrier mobility and current on-off ratio at room temperature, has attracted much more attentios recently [10]. However, the electrical performance of InSe-based devices suffered severe degradation because the InSe channels are extremely unstable under ambient conditions (physical absorption of the H_2O or O_2) [11–13]. Various

passivation techniques such as h-BN, PMMA, or high-k oxides have been used to improve the stability of InSe-based devices in ambient environments [14]. InSe is comprised of vertically stacked Se-In-In-Se layers with weak van der Waals interactions. The bandgap energy of InSe increases from 1.25 eV for bulk to 1.89 eV for bilayer due to the strong quantum confinement in 2D InSe [15]. A weak locally resolved PL signal at about 2.14 eV is also observed in monolayer InSe obtained by using a solution-processable method [16] and a mechanical exfoliation approach, [17] respectively. These unique properties make InSe an ideal candidate for a channel material in next-generation electronic and optoelectronic devices.

In-depth understanding of the underlying mechanism of how temperature affects the lattice structure and the electrical properties will provide the fundamental insight for improving InSe device performance in the future. Significant progress has been made on predicting the temperature effect of the structural or the electrical properties. Errandonea *et al* demonstrated the phase transition from the rhombohedral polytype to the monoclinic phase of InSe under high-pressure and high-temperature by optical measurements [18]. Huang *et al* reported the mobility of InSe field-effect transistors (FETs) as a function of temperature from 2 to 250 K, which shows the mobility increases with decreasing temperature and saturates at a constant value for temperature less than 20 K [19]. However, there is a lack of simultaneous analysis on the temperature dependence of the lattice structure behavior in InSe semiconductors and the electrical performance of related devices.

In this letter, detailed vibrational modes of layered InSe and the electronic properties of 3 nm indium-deposited InSe FETs as a function of temperature have been investigated. The difference of phonon frequency ($\Delta\omega$) for the A^2_{1g} mode is found to be larger than that of the E^1_{2g} mode due to the stronger electron-phonon coupling for the A^2_{1g} mode. Furthermore, the electron-doping behavior at the In/InSe interface is proved by surface potential characterization and the energy band structure analysis. Moreover, FETs dependent on the temperature and the InSe thickness, as an applicable device, are designed. Our findings can promote comprehensive consideration on how to enhance the performance of temperature-variant InSe based devices in future.

2. Experimental details

Layered InSe nanosheets were mechanically exfoliated from a bulk InSe crystal (2H ε-stacking phase) on heavy *p*-doped Si wafers with a 300 nm thick SiO_2 layer. Here, the terminal of Si acts as the back-gate, and the SiO_2 layer acts as the dielectric layer. A 3 nm thick indium layer was deposited on top of the whole InSe nanosheet. The electrical contacts were obtained by evaporating 50 nm thick Au through a commercial shadow mask. The thickness and surface potential details of the InSe nanosheets were investigated by atomic force microscopy (AFM) and Kelvin probe force microscopy (KPFM) techniques (Bruker, Dimension Icon SPM), respectively. Temperature-dependent Raman spectra were carried out using a Jobin-Yvon LabRAM HR Evolution spectrometer (λ: 532 nm) and a THMSE 600 heating/cooling stage (Linkam Scientific Instruments) at the temperature range of 80-295 K with a resolution of 0.1 K. The electronic properties of the InSe FETs were measured with a Janis ST-500 cryogenic probe station with a Keithley 4200-SCS semiconductor parameter analyzer.

3. Results and discussion

Figure 1(a) depicts the optical image of InSe flakes ranging from 5 to 24 layers. The thickness of InSe flakes is measured by AFM as well as the method of evaluating optical contrast. Raman spectroscopy is a very appropriate and advanced technique to characterize the structural, optical and mechanical properties of layered materials such as graphene, MoS_2, WSe_2, $MoTe_2$, WTe_2, black phosphorus, TiS_3 and other layered materials [20–24]. The Raman spectroscopy technique is widely used to provide detailed information about the composition and the molecular vibration behavior of two-dimension materials by frequency shift and peak broadening with high resolution. As we know, clarifying molecular vibration behavior in 2D materials is important to study the electron-phonon interactions, transport properties and crystal structure of materials, which play a key role in the electronic performance of nanodevices, especially in the charge carrier mobility [25–28]. The inset in figure 1(b) shows the AFM topography with a height spectrum of the 4.6 nm thick InSe prepared for scattering collection. Figure 1(b) represents the typical Raman shift of few-layer InSe as a function of the temperature. It is clear to see that there is a redshift trend in the peak positions with increasing temperature. An increase in the full width at half maximum (FWHM) of the peaks is observed for the InSe nanosheet with increasing temperature. Apparently, the temperature dependence of the Raman spectra of the few layer InSe is similar to that of graphene [29, 30]. Furthermore, the main phonon vibrations of the InSe nanosheet at room temperature are obtained at about 115, 178, 199 and 227 cm^{-1}, which can be assigned to the A^1_{1g}, E^1_{2g}, A^1_{1g}(LO) and A^2_{1g} modes, respectively [18]. The Raman spectra of few-layer InSe flakes exhibit a strong peak at 199 cm^{-1}, which is a marker of the ε phase, as indicated by earier works on InSe [31, 32]. The A^1_{1g}(LO) mode in the spectra may be explained by the following two sets: the polar mode intensity is related to light absorption of InSe; the interaction between polar phonons and $E^{'}$ transition induced electron-hole pair generation [33]. The $E^{'}$ transition, which is the energy difference between the lowest conduction band and second highest valence band [33].

Figure 1(c) and (d) demonstrate the typical plots for the Raman spectra peak positions as a function of the temperature for the InSe nanosheets. In (I) and (II), the thickness of InSe flakes are 4.6 nm and 8.6 nm, respectively. The Raman modes for InSe nanosheets behave linearly with the temperature ranging from 80 K to 295 K. The Raman phonon frequency as a function of the temperature is fitted by the following formula: $\omega(T) = \omega_0 + \chi T$ [26]. Where ω_0 is the phonon frequency of the A^1_{1g}, E^1_{2g}, A^1_{1g}(LO) and A^2_{1g} modes at zero

Kelvin temperature, χ is the first-order temperature coefficient of each main mode. The temperature coefficient χ comes from the slope of the fitted straight line. Figure 1(c) demonstrates that the calculated value of temperature coefficient χ for the E^1_{2g} and A^2_{1g} modes corresponding to 4.6 nm and 8.6 nm InSe nanosheets are -0.011 $cm^{-1}K^{-1}$, -0.014 $cm^{-1}K^{-1}$ and -0.013 $cm^{-1}K^{-1}$, -0.014 $cm^{-1}K^{-1}$ respectively. The change in the Raman modes with the temperature is mostly due to anharmonicity, which is related to anharmonic contributions to the interatomic potential energy mediated by phonon-phonon interactions. The value of $\Delta\omega$, corresponding to the A^2_{1g} mode is found to be 3.14 cm^{-1}, which is larger than that of the E^1_{2g} mode (2.47 cm^{-1}) in the 4.6 nm InSe nanosheet. It is attributed to the electron-phonon coupling for the A^2_{1g} mode being stronger than that of the E^1_{2g} mode. Furthermore, the value of $\Delta\omega$ for the E^1_{2g} mode (3.09 cm^{-1}) in the 8.6 nm InSe nanosheet is larger than that of the 4.6 nm InSe flake. It may result from the stronger strain in the thicker InSe nanosheet. Figure 1(d) demonstrates that the frequency of the A^1_{1g} and A^1_{1g}(LO) mode corresponding to 4.6 nm and 8.6 nm InSe are measured to be 115.25 cm^{-1}, 200.26 cm^{-1} and 115.53 cm^{-1}, 200.24 cm^{-1}, respectively. As thickness decreases, the frequency of the A^1_{1g} mode decreases and that of the A^1_{1g}(LO) mode increases. The blue-shift of the A^1_{1g} mode with decreasing thickness arises from the stronger In-Se bond in thinner layers. The stronger bond gives rise to a higher frequency of vibrations. However, the gradually weakened interlayer interaction of In-In bonds leads to the decreasing frequency of the A^1_{1g} mode. Furthermore, as the temperature decreases, a distinguished peak appears at 209 cm^{-1}, which is assigned as the polar mode E(LO). [34–36] This phenomenon may arise from the dominant intraband Fröhlich electron-phonon interactions, which originate from the scattering of electrons or holes within the same band by the macroscopic electric field of a LO phonon [37]. Furthermore, with increasing temperature, an increase in the FWHM of the peak is observed for the InSe nanosheet as shown in figure 1(e). The change in line width as a function of temperature is given by the equation:[38]

$$\Gamma(T) = \Gamma_0 + A[1 + n(\omega_1, T) + n(\omega_2, T)] \quad (1)$$

where Γ_0 represents the background contribution, A and $n(\omega,T)$ are the anharmonic coefficient and the Bose–Einstein contribution function, respectively. The temperature dependent FWHM can be determined from the parameters such as Γ_0, A, ω_1 and ω_2. The broadening in FWHM with temperature is mainly attributed to the contribution from the decay of a zone center optical phonon into one acoustic and one optical phonon.

Towards understanding the electrical characteristics of the InSe nanosheet, back-gated FETs are fabricated. The insets of figure 2(a) show the schematic and optical images of a typical 3 nm indium-deposited InSe FET nanodevice, respectively. Figures 2(a) and (c) demonstrate the transfer characteristics ($I_{ds} - V_{bg}$) of this well-fabricated InSe FET with/without indium deposited at different V_{ds}. Note that it indicates a typical *n*-type behavior with a high on/off current modulation of more than 10^6. Furthermore, the observed loop curves exhibit weaker hysteresis in the InSe FET deposited 3 nm indium than that in the InSe FET without indium deposited, and gradually reduce with the V_{ds} increasing. It also demonstrates the effective surface protection for the InSe channel after the deposition of the indium layer. The corresponding output characteristics ($I_{ds} - V_{ds}$) for the indium-deposited/without indium deposited InSe FET are plotted in figures 2(b) and (d), which also confirm an excellent Ohmic contact between the layered InSe conducting channel and the metal indium interface in the indium-deposited InSe FET. More than 30 layered InSe FETs were synthesized and analyzed statistically to confirm the validity of this study. Furthermore, when comparing the transfer characteristic (figure 2(a)) with the output characteristic (figure 2(b)), clear hysteresis is shown in the transfer characteristic. The observed hysteresis loop in the transfer characteristic is derived from the interfacial trapping states between the InSe channel and SiO_2 dielectric layer.

It is necessary to give further explanation on the performance of the 3 nm indium-deposited InSe FET by comparing differences between the heterostructure of the InSe and the 3 nm indium-deposited InSe (In/InSe). Figure 2(e) maps the topography and the discrepant contact potential difference (*CPD*) distribution on the heterostructure recorded by KPFM, which is widely employed to probe the local variations of work function distribution on heterostructure [39]. The *CPD* value between the KPFM tip and the local contact area of InSe or In/InSe can be expressed as

$$CPD_{InSe} \times e = W_{tip} - W_{InSe} \quad (2)$$

$$CPD_{In/InSe} \times e = W_{tip} - W_{In/InSe} \quad (3)$$

where W_{tip}, W_{InSe} and $W_{In/InSe}$ are the surface work functions of the tip, InSe and In/InSe, respectively. [40] The $CPD_{In/InSe}$ value is less than that of the CPD_{InSe}, as shown in figure 2(e). According to equations (2) and (3), the measured work function of the In/InSe is larger than that of the InSe. It is noted that the larger work function of In/InSe can be beneficial to the charge transfer from the Au electrode to the InSe conduction channel. On the other hand, we further investigate the energy band structure before and after depositing the indium layer in contact with the top of the InSe semiconducting channel, as depicted in figure 2(f). The work function of indium is about 4.12 eV, which is lower than that of InSe (4.7 eV) [41, 42]. When indium is deposited on top of the InSe layer, the electrons flow from the indium layer into the InSe conduction channel in order to reach thermal equilibrium. With the gradual accumulation of the electrons on the InSe surface, the conduction band E_c near the InSe surface can bend downward. The band bending in In/InSe effectively makes the semiconductor surface appear more *n*-type than the case without deposition, leading to higher surface charge density at the interface.

Except for illustrating the improvement of indium deposition on InSe FET performance, we study the 3 nm indium-deposited InSe FETs with different layer thickness of InSe

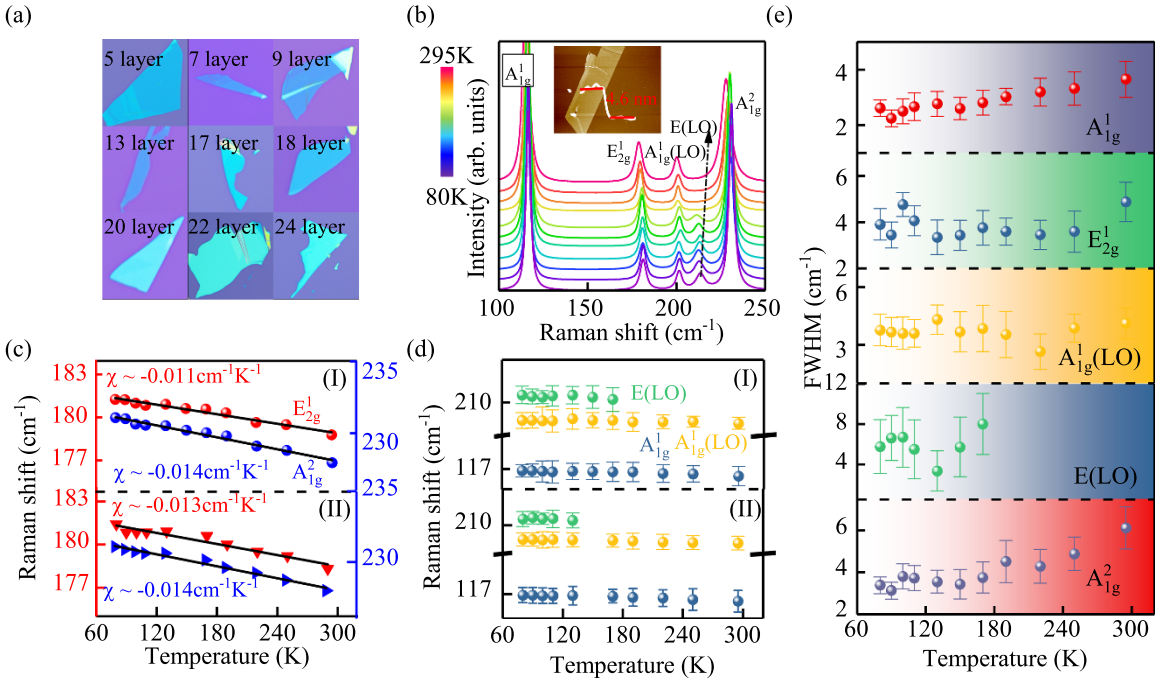

Figure 1. (a) Optical images of the InSe flakes. The thickness ranges from 5 to 24 layers. (b) Temperature dependent Raman spectra of a InSe nanosheet, the corresponding modes are denoted as A^1_{1g}, E^1_{2g}, A^1_{1g}(LO), E(LO), A^2_{1g} modes, respectively. Inset: AFM image showing a height difference of 4.6 nm. (c) and (d) are the evolution of the phonon frequency for the InSe nanosheet under temperature from 80 K to 295 K. In (I) and (II), the thickness of InSe flakes are 4.6 nm and 8.6 nm, respectively. (e) The FWHM of the modes in the 100–250 cm^{-1} as a function of the temperature.

flakes. Figure 3(a) provides the transfer characteristics as a function of the InSe thickness for the InSe FET, which are measured from −60 V to 60 V with the same sweeping rate at room temperature. As the thickness of the InSe nanosheet decreases, the transfer behaviors of the InSe FETs follow similar trends and obviously shift towards higher gate voltages. The slope of the transfer curves exhibit distinct changes. It implies that the threshold voltage and subthreshold slope (SS) are significantly affected by the thickness of the InSe nanosheet. The SS is an important parameter in the subthreshold region, which describes how the transistor-based device opens and closes [43, 44]. SS is defined by the equation: $SS = dV_{bg}/d(\log I_{ds})$, where the logarithm is in base 10. SS can be obtained directly from the curve of $-I_{ds}$ versus V_{bg} on a logarithmic scale, which represents the change speed of the on/off switching of the transistor-based device. The calculated SS of 9, 17 and 20 layer InSe FETs are 120, 184 and 254 mV $decade^{-1}$, respectively. Furthermore, the threshold voltages of the 9, 17 and 20 layer InSe FETs are 16.44, −18.7 and −20.11 V, respectively. The threshold voltage was found to shift to a more negative V_{bg} with the thickness increasing. Additionally, the carrier density is calculated using the equation of $\Delta n_{2D} = C_g \Delta V_{peakshift}/e$, where Δn_{2D} and e are the carrier density variation and elementary charge, respectively. C_g is the oxide capacitance of 11.5 $nFcm^{-2}$; $\Delta V_{peakshift}$ is the voltage shift as a function of the thickness for the corresponding transfer characteristics [45]. The calculated values of Δn_{2D} for the thickness of the InSe increasing from 9 to 17 layers is about 2.53×10^{13} cm^{-2}, which is larger than that of the thickness increase from 17 to 20 layers (1.01×10^{11} cm^{-2}). Note that the carrier density variation decreases as the thickness of the InSe larger than 17 layers. The corresponding output characteristics of the same devices are shown in the figure 3(b). It can be observed that the linearity characteristic of all output curves implies an Ohmic contact between the layered InSe conducting channel and the indium deposition. To characterize device performance, the mobility of InSe FETs is also extracted from the transfer curve using the following equation [50]

$$\mu_0 = \frac{1}{C_i} g_m \frac{L}{W} \frac{1}{V_{ds}} \tag{4}$$

where $C_i = \frac{\varepsilon_0 \varepsilon_r}{d}$, ε_0 is 8.854×10^{-12} Fm^{-1}, ε_r for SiO_2 is 3.9, d is the thickness of SiO_2 (300 nm), the value of the oxide capacitance C_i is about 11.5 $nFcm^{-2}$, L is the channel length of the FETs, W is the channel width of the FETs, V_{ds} is the drain to source bias, and $g_m = dI_{ds}/dV_{bg}$ is the transconductance. Field effect mobility values of the FETs dependent on the thickness of the InSe nanosheets at $V_{ds} = 0.1$ V are shown in figure 3(c), the values of the quantities used in the calculations are shown in the table 1. Note that the mobility increases as the layer thickness of InSe from 7 to 17 layers, and then decreases from 17 to 38 layers. Similar thickness dependence of carrier mobility is also observed in MoS_2 and graphene [46, 47]. The mobility decreases with the thickness decreasing from 17 to 7 layers. It can be explained by the following: a thin native oxide is progressively formed when exposed to an ambient enviroment, forming charge traps at the InO_x/InSe interface with poor screening; [48] in an oxide insulator like

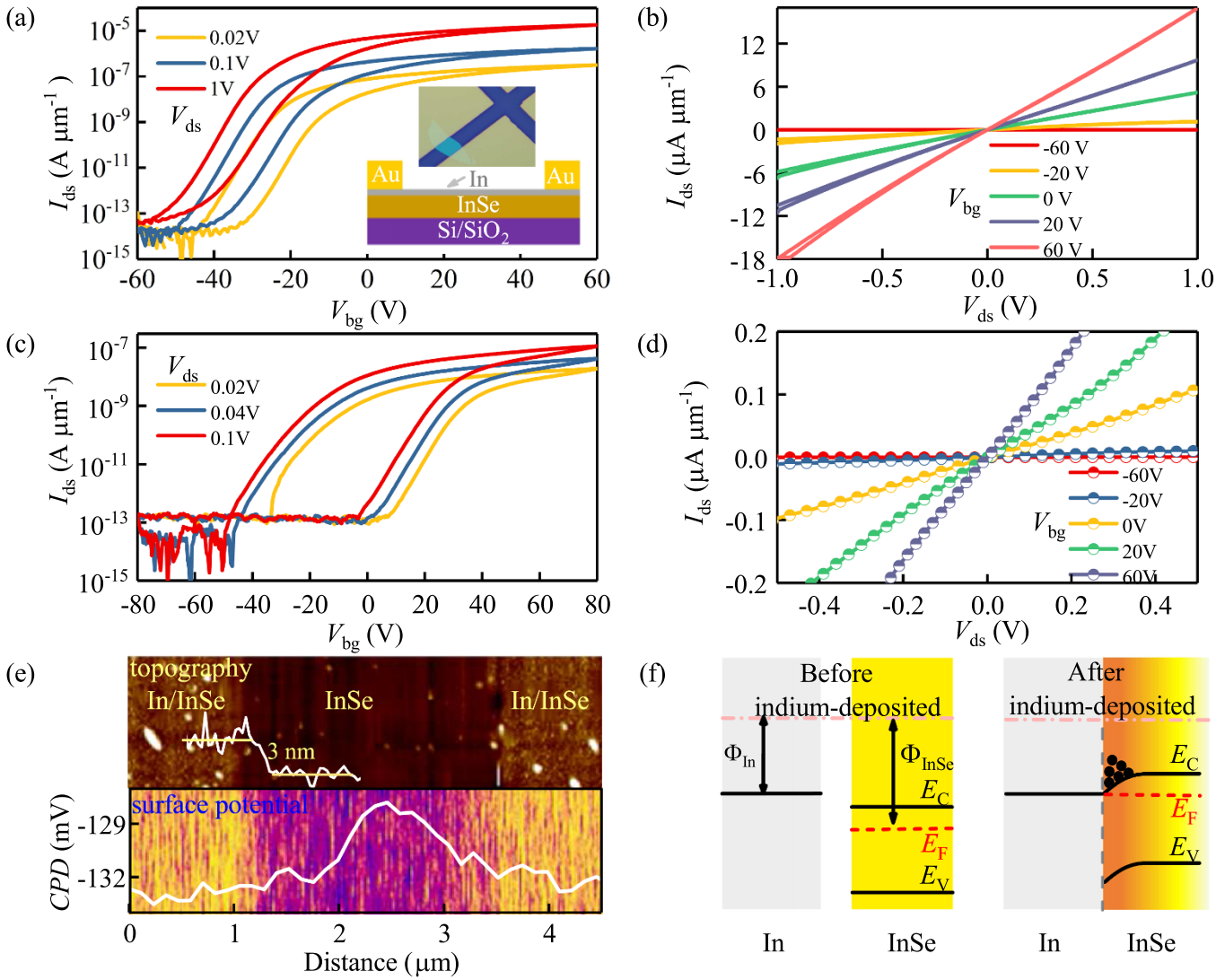

Figure 2. (a) The transfer characteristics of a layered InSe FET with 3 nm thick indium layer at different V_{ds}. Lower inset shows schematic of back-gated thin-film InSe FETs consisting of a SiO_2 back-gate insulator(300 nm). And upper one is optical image of a fabricated thin-film InSe FET. (b) Output characteristics of the indium-deposited InSe FET at various V_{bg}. (c) The transfer characteristics of a layered InSe FET without any indium deposited at different V_{ds}. (d) Output characteristics of the InSe FETs without indium-deposited at different V_{bg}. (e) AFM topography with a line profile in height, and the built-in potential distributions with a line scan at the InSe and InSe with 3 nm thick indium layer, respectively. (f) Schematic illustrations of the energy band structure before and after depositing an indium layer on top of the layered InSe semiconducting channel.

SiO_2, the metal-oxide bonds are easily polarized and the oscillatory motion of these bonds from the polar phonon modes produces a time-dependent evanescent field at the substrate that can scatter electrons in the InSe [49]. The reduction of mobility after 17 layers can be explained by the Thomas-Fermi charge screening theory, when the thickness of the InSe FET is less than the largest thickness of the space charge region (L_D) [50]. The largest thickness of the space charge region can be expressed by $L_D = \sqrt{\frac{\varepsilon_s \varepsilon_0 k_0 T}{q^2 N_0}}$, where ε_s is the dielectric constant of the semiconductor material, ε_0 is the vacuum permittivity, k_0 is the Boltzmann constant, T is thermodynamic temperature, N_0 is the equilibrium carrier concentration, and L_D is called the Debye screening length. Where the thickness of the sample is less than L_D, the sample works as an intralayer resistance; as a result, the current can easily be injected from the top contacts under the regulation of the gate voltage. But, when the thickness of the sample is larger than L_D, the gate voltage hardly affects the top layers of the sample. Both the interlayer resistance and the intralayer one are very important.

However, the working temperature is considered as the critical factor on the electrical properties of InSe nanosheets. The mobility as a function of the temperature can be useful for the identification of the main scattering mechanisms and helps to find the optimal value of the intrinsic electron-phonon couplings [51]. To obtain a better insight into the mechanism of temperature effect on the FET performance, we implement the FET properties in a temperature range of 80–320 K. Figure 4(a) shows the transfer curves as a function of temperatures on a indium-deposited InSe transistor. The thickness of the InSe nanosheet corresponding to the FET is about 24.6 nm. As the temperature increases, the threshold voltage V_{th} of the device moves towards the negative direction. The

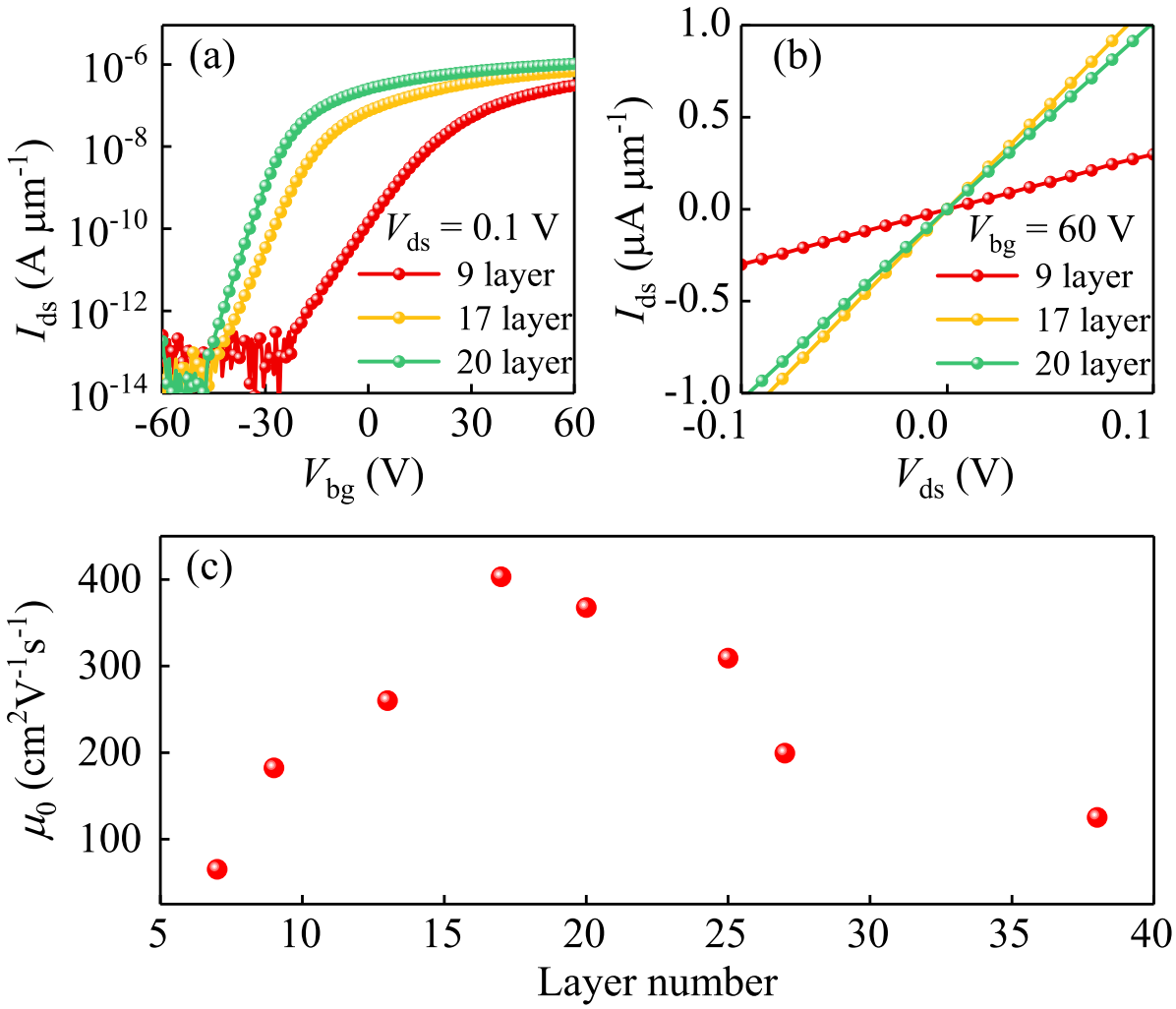

Figure 3. (a) and (b) are the thickness dependence of the transfer and output characteristics of indium-deposited InSe FET. (c) Carrier mobility as a function of the thickness for InSe FET.

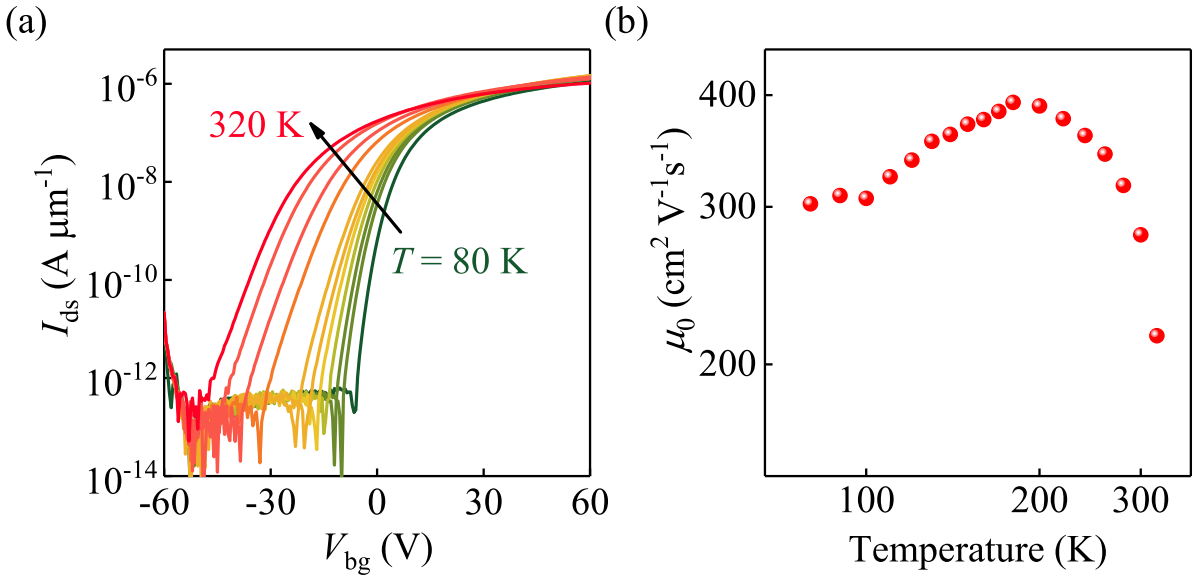

Figure 4. (a) Transfer characteristic of the indium-deposited InSe FET as a function of temperature under the V_{ds} = 0.1 V. (b) Temperance dependence of carrier transport under the V_{ds} = 0.1 V.

Table 1. The field effect mobility values of the few-layer InSe FETs

Thickness (layer)	μ_0 ($cm^2V^{-1}s^{-1}$)	L (μm)	W (μm)	Gm (S)
7 L	65.28	14.9	11.91	6×10^{-8}
9 L	182.45	15.91	3.49	4.6×10^{-8}
13 L	259.95	13.81	12.47	2.7×10^{-7}
17 L	403.02	18.8	6.08	1.5×10^{-7}
20 L	367.64	11.29	6.09	2.28×10^{-7}
25 L	309.09	15.27	14.95	3.48×10^{-7}
27 L	199.34	14.43	9.442	1.5×10^{-7}
38 L	125.07	15.05	31.39	3×10^{-7}

specific values of mobility in figure 4(b) clearly show a monotonous increase of the mobility as the temperature decreases near 180 K. After the mobility reaches the highest value at around 180 K, it decreased at lower temperatures. Accordingly, the carrier mobility could be also qualitatively recognized by ionized impurity scattering or acoustic phonon scattering [52]. At high temperature values (>180 K), the mobility increases as the temperature decreases, which may be mainly attributed to the phonon scattering. At lower temperature values (<180 K), the mobility decreases with the decreasing of temperature. Such behavior may be ascribed to the impurity scattering in the material (scattering from ionized impurities). Therefore, the temperature dependence of InSe based FET performance is closely consistent with the structural findings from studying the phonon vibrational modes by Raman scattering.

4. Conclusion

In summary, we systematically investigated the temperature dependence of the crystalline structure and electrical performance of layered InSe FET devices. Analyses of Raman spectra suggest that the difference of phonon frequency for the A_{1g}^2 mode is found to be larger than that of the E_{2g}^1 mode due to the stronger electron-phonon coupling for the A_{1g}^2 mode. Furthermore, the device performance based on indium-deposited InSe is highly dependant on the electron-doping behavior at the In/InSe interface and the predicted energy band structure. FETs are designed considering the temperature and thickness of InSe flakes as the applicable device. This study will promote further understanding of the underlying physics in the relationship between the crystalline structure of a 2D material and the performance of the developed nanodevice.

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