AIP Advances

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Cite as: AIP Advances **9**, 085031 (2019); https://doi.org/10.1063/1.5112078
Submitted: 02 June 2019 . Accepted: 21 August 2019 . Published Online: 28 August 2019

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ABSTRACT

Static characteristics of digital combinational logic circuits and Schmitt triggers based on two-dimensional (2D) transition metal dichalcogenides (TMDs) have been systematically explored. Selenide tungsten (WSe_2) transistors act as the P type metal oxide semiconductor (PMOS). Molybdenum disulfide (MoS_2) transistors play the role as N type metal oxide semiconductor (NMOS). Based on the circuit simulations, we find that the output of the complementary metal oxide semiconductor (CMOS) inverters and Schmitt triggers can approach the supply voltage (VDD) and ground (GND), respectively. The key performance indexes of the two digital circuits have been studied with the change of the device parameters. The simulation results indicate that a thinner gate oxide thickness and a higher dielectric permittivity gate oxide material can increase the noise margin of the inverters. Besides, different width ratios of PMOS and NMOS can influence the noise margin of inverters. An inverter with a large PMOS whose width is 64 nm and a small NMOS whose width is 32 nm can improve the low level noise margin, but reduce the high level noise margin. In addition, a gate oxide thickness of 2.8 nm can broaden the hysteresis window of the Schmitt triggers obviously. The output curves of the Schmitt triggers change slightly with different gate oxide materials. The hysteresis window of the Schmitt triggers becomes narrow with decreasing of the supply voltage. The present work could help to design the standard cells with different requirements and improve the performance of digital integrated circuits using TMDs transistors.

I. INTRODUCTION

Two-dimensional transition metal dichalcogenides (2D-TMDs) field effect transistors (FETs) have been seen as the candidate in the next generation of semiconductor industry for its excellent electrical properties. However, it still lacks further study in optimization of TMDs FETs based digital integrated circuits. Since the first discovery of graphene in 2004, two-dimensional layered materials have been widely researched in their unique and excellent physical, electrical, optical and mechanical characteristics.[1–3] The electron mobility of graphene can reach above 5000 $cm^2/V\,s$.[4] However, the narrow bandgap of graphene leads to a large turn off current. Thus, graphene can hardly take place of silicon in semiconductor industry. At this point, a variety of other layered materials had been discovered, such as transition metal dichalcogenides (TMDs).[5] Molybdenum disulfide (MoS_2) is a typical TMDs. Unlike graphene, the bandgap of MoS_2 can change from 1.3 to 1.9 eV for its different thicknesses.[6–10] Besides, researchers found that MoS_2 transistors show the N type behavior due to the sulfur vacancy defect. On the contrary, another typical TMDs, selenide tungsten (WSe_2), was found to have hole injection, which indicates that WSe_2 FETs show the characteristics of P type transistors.[11]

MoS_2 FETs were first fabricated on SiO_2 substrates with HfO_2 as the gate oxide material.[12] The subthreshold slope of the MoS_2 FETs were measured to be almost 74 mV/decade and the on/off current ratio is nearly 10^8 at room temperature. Later, researchers have drawn their attentions on the fabrication of circuit designs using TMDs FETs.[11,13,14] The CMOS inverters made up of only one channel material have been discussed in some literatures.[15,16] In their works, they used the N type doped WSe_2 as the NMOS channel material and the P type doped WSe_2 as the PMOS channel material. Besides, some simulation works were also done to find out the performance of integrated circuits before fabrication. In 2016, simulations concerning on the impacts of supply voltage, materials, and mechanical bending on delay of digital circuits have been conducted.[17] Besides, Wei *et al.* have explore the relationship between analog design metrics and the device level characteristics during analytical derivation and numerical simulations.[18]

To be compatible with current electronics design automation (EDA) tools such as HSPICE, many researchers focus on the electrical behavior of TMDs FETs and device simulation models such as spice model.[19] David Jimenez used the traditional drift-diffusion theory to study the leakage current and surface potential models of single-layer TMDs transistors. This model is suitable for long channel length and low power consumption.[20] When the channel length is reduced to below 20 nm, the ballistic transport model can more accurately illustrate the transport of carriers.[18] Due to the large amount of calculation of the ballistic model and the complicated calculation process, the cost of time increased and the speed of the EDA tools became slower. Therefore, quasi-ballistic models were proposed.[17,19,21,22] They are accurate enough when used in circuit design simulations with TMDs FETs whose channel lengths are above 15 nm.

Overall, the studies above fixed attention on the on/off current ratio, subthreshold slope, delay and some analog design metrics. However, the static characteristics of digital circuits are still undiscussed in detail. In order to design a better digital circuit, a series of standard cells with different static characteristics are needed. The relationships between device physical parameters and static characteristics of digital circuits remain large unexplored.

In this work, we focus on the static characteristic of CMOS inverters and Schmitt triggers using TMDs FETs. Besides, the influences of the device parameters on the noise margin of the CMOS circuits are also studied in the present work. The simulation results can help to optimize the structure of TMDs FETs transistors and improve the performance of TMDs FETs transistors based digital circuit design. We choose the compact model[17] and the corresponding Verilog-A model[22] to run the circuit design simulations. This compact model fits well with the HSPICE simulator and corresponds with the non-equilibrium Green's function (NEGF) date[23] and the experimental data.[12,24]

II. EXPERIMENTAL DETAILS

The quasi-ballistic compact model adopted in this work was based on the drift-diffusion model. The drain current of the TMDs FETs can be expressed as follow:

$$I_D = BEF * W * C_{ox} * (V_G - V_T) * V_{sat} * \frac{1-R}{1+R} \quad (1)$$

Where W is the effective channel length. C_{ox} is the top gate oxide capacitance. V_g is the bias voltage applied on the top gate. V_T is the threshold voltage, which refers to the minimum turn-on voltage. V_{sat} is the saturation velocity, which can be affected by channel length and the bias voltage of source and drain. R is the backscattering coefficient and can be theoretically computed by

$$R = \frac{l}{1+\lambda} \quad (2)$$

Where l is the critical distance and λ is the mean free path. BEF is the ballistic enhancement factor and depends on the bias voltage of source and drain, which can be expressed as

$$BEF = \gamma_1 * V_G + \gamma_2 * V_D \quad (3)$$

In which, γ_1 and γ_2 are the fitted coefficients, V_D is the bias voltage of drain.[17]

Fig. 1(a) shows the schematic of the inverter. When the input of the inverter is high, the MoS_2 transistor is turned on and the WSe_2 transistor is turned off. So the output connects with ground through the MoS_2 transistor and the output is low. On the contrary, when the input is low, the WSe_2 transistor is turned on and the MoS_2 transistor is turned off. So the output connects with the supply power through the WSe_2 transistor and the output is high. Thus, the reverse behavior is achieved. For the inverter, we can get the following equation through the circuit structure.

$$I_{DN} = -I_{DP} \quad (4)$$

$$V_{GN} = V_{GP} = V_{in} \quad (5)$$

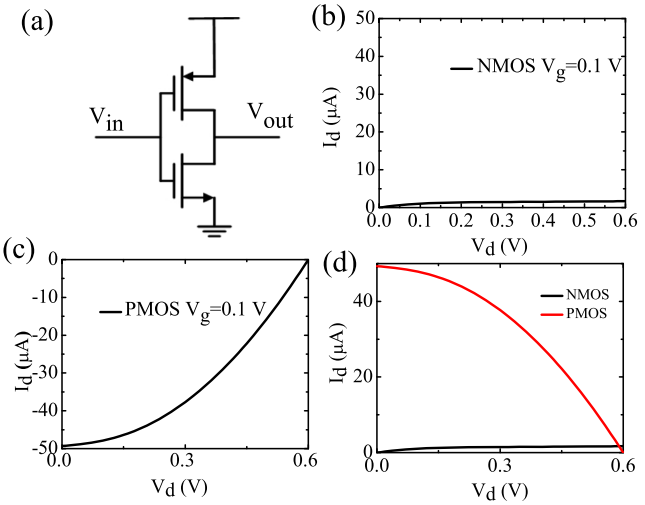

FIG. 1. (a) The schematic of inverters. The PMOS channel material is WSe_2 and the NMOS channel material is MoS_2. (b) The drain current of MoS_2 when V_g=0.1V. (c) The drain current of WSe_2 when V_g=0.1V. (d) The intersection of $I_d - V_d$ curve of NMOS and the processed $I_d - V_d$ curve of PMOS, its x-coordinate refers to the output voltage of the inverter when V_{in} is 0.1V.

$$V_{DN} = V_{DP} = V_{out} \tag{6}$$

Substituting the equation (1) (5) (6) into the equation (4) we can get the following formula:

$$BEF_N * W_N * C_{oxN} * (V_{in} - V_{TN} * V_{satN} * \frac{1 - R_N}{1 + R_N} = -BEF_P * W_P * C_{oxP} * (V_{in} - V_{TP} * V_{satP} * \frac{1 - R_P}{1 + R_P}) \tag{7}$$

To obtain the voltage transfer characteristics (VTC) curve of the inverter, the gate voltages of the two transistors are set to V_{in}. The drain voltages of the two transistors are set to V_{out}. Then we take the absolute value of the drain current I_d of WSe_2 and draw the processed I_d in the same coordinate with the I_d of NMOS. The intersection of the two curves shows the output voltage of the inverter. As shown in Fig. 1, we take V_{in}=0.1V as an example. Fig. 1(b) and (c) show the $I_d - V_g$ curve of MoS_2 and WSe_2, respectively. In Fig. 1(d), the absolute value of the drain current of WSe_2 and the I_d of MoS_2 are drawn together in the same coordinate. The x-coordinate of the intersection is the corresponding output voltage, where we can see that the output voltage is nearly 0.6 V. Next, different V_{in} values were taken to obtain the corresponding intersections. At last, all the intersections make up the output characteristic curve of the inverter.

III. RESULTS AND DISCUSSION

A. Factors affecting the performance of inverters using TMDs FETs

CMOS inverters are the most commonly used combinational logic circuits in digital integrated circuits. They are the basis of digital integrated circuit design, and its performance and quality are critical to digital integrated circuit design. We use a single layer MoS_2 transistor as the NMOS transistor and a single layer WSe_2 transistor as the PMOS transistor.

The noise margin of digital circuit reflects the performance of the digital design when it works under noise conditions. The maximum output voltage is called as output high voltage (V_{OH}). The minimum output voltage is called as output low voltage (V_{OL}). The input voltages corresponding to the unity gain point are defined as the allowed critical level. That is, the point where the slope of the transfer characteristic curve is -1 will be recorded as V_{IL} (the lower input point) and V_{IH} (the higher input point). When the input signal is less than V_{IL}, the input will be treated as low level. When the input signal is greater than V_{IH}, the input will be treated as high level. The input signal will be regarded as invalid input if it is between V_{IL} and V_{IH}. Therefore, the smaller the difference between V_{IL} and V_{IH}, the better the performance of the inverter. Considering that only one transistor of the CMOS inverter is on at a time, V_{OH}=VDD and V_{OL}=GND. Thus, the noise margin of the logic high level is: $N_{MH}=V_{OH} - V_{IH}$=VDD-V_{IH}, and the noise margin of the logic low level is: $N_{ML}=V_{IL} - V_{OL}=V_{IL}$.[25]

As shown in equation (7), the VTC curves of inverters vary with the gate oxide thickness, the gate oxide material and the size of the device change. Thus, we explore the effects of these device parameters on the VTC curve and noise margin of inverters. Fig. 2 presents the simulation results. As we can see, with a thinner gate oxide, V_{IL} shifts to right and V_{IH} shifts to left. Thus, we will get an inverter with a large noise margin if we choose a thinner gate oxide. A thinner gate oxide makes the distance between the two plates of the capacitor shorter and leads to a larger gate capacitance. Thus, a smaller threshold voltage will be obtained and help the gate control the drain current more effectively. Besides, we can conclude that, for typical gate oxide materials (HfO_2, Al_2O_3 and SiO_2), the VTC curves change with the dielectric permittivity of the gate oxide materials. Moreover, we can see that a higher dielectric permittivity of the gate oxide material leads to a higher V_{IL} and a lower V_{IH}. The reason for this phenomenon is that a high-K material can provide a larger capacitor and more effective gate control capability under the same conditions. As shown in Fig. 2(c), an inverter with a larger NMOS whose width is 64 nm and a small PMOS whose width is 32 nm will be a pull-down device. On the contrary, when a pull-up inverter is needed, the inverter with a large PMOS whose width is 64 nm and a small NMOS whose width is 32 nm can meet the requirement.

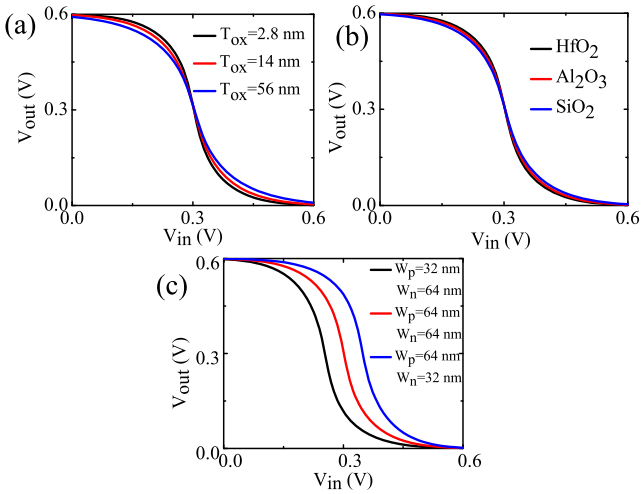

FIG. 2. Output curves of inverters change with different device parameters. (a) gate oxide thickness, (b) gate oxide material (different gate oxide dielectric permittivity), (c) the width of devices.

B. Factors affecting the performance of Schmitt triggers using TMDs FETs

Another digital circuit studied in our work is Schmitt triggers, which is also known as Schmidt inverters. Fig. 3(a) gives one of the typical schematic of Schmitt triggers. They exhibit a special hysteresis characteristic on the output curve due to their positive feedback. The switching threshold of Schmitt triggers is variable and depends on the direction of the flip. That is, when the input signal goes from a low voltage, the corresponding switching threshold is different from that when the input signal falls from a high level. In addition, Fig. 3(b) indicates that the edge of the output waveform becomes steeper, as compared with the inverter. The two characteristics help Schmitt triggers perform better than inverters under the noisy environments. The two characteristics also help reduce the transition delay time of digital signals.[25]

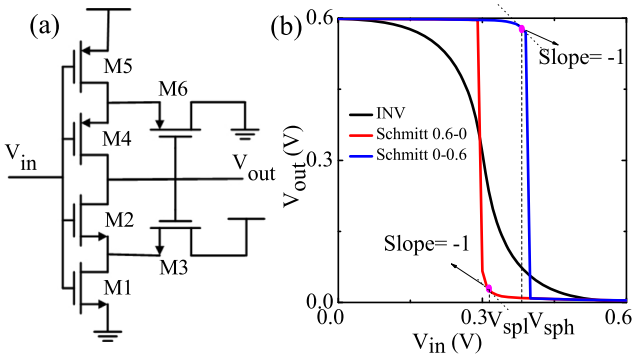

FIG. 3. (a) Schematic of Schmitt triggers. (b) Output curve of Schmitt triggers compared with that of an inverter.

From the structure of the Schmitt triggers, we can conclude that when the V_{in} is in low level and the V_{out} is in high level, the NMOS (M1, M2) and the PMOS (M6) are off, the PMOS (M4, M5) and the NMOS (M3) are on. V_{out} connects to supply voltage through M4 and M5, and the voltage of the source of M2 (V_{s2}) is VDD-V_{ds3}. V_{ds3} is the voltage between the source and drain of M3. With increasing of V_{in}, M1 will turn on when V_{in} reaches its threshold voltage and V_{s2} begins to fall. As V_{in} increases and let M2 meet its threshold voltage and turns on, the output begins to fall down to ground and M3 starts to turn off. That is where we define the voltage of the high switching voltage, which is called V_{sph} and can be expressed as $V_{sph}=V_{s2}+V_t$. With the cutoff of M3, V_{s2} will fall even more, which in turn makes M2 turn on even more. When M3 turns off completely and M1 and M2 turn on, the positive feedback ends. The positive feedback confirms the switching voltage of the Schmitt triggers. It can be analyzed with the same methods when the input is high and the output is low. Fig. 3(b) gives the output curve of the Schmitt triggers and the inverter applying TMDs FETs, respectively. We can see that the output curve is steeper, as compared with the inverter. The switching voltage is better than the inverter, which is corresponding to the above discussion.

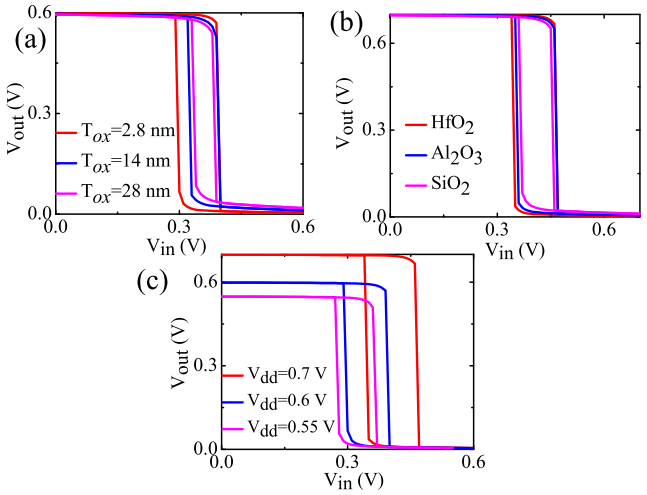

FIG. 4. Output curve of Schmitt triggers changes with different device parameters. (a) gate oxide thickness, (b) gate oxide material (different gate oxide dielectric permittivity), (c) supply voltage.

To explore how different device parameters influence the switching voltage of Schmitt triggers, we simulate the same circuit configuration with several gate oxide thicknesses, three kind of typical gate oxide materials and various supply voltages. From Fig. 4(a), we can see that with increasing of the gate oxide thickness, the V_{spl} and V_{sph} shift to the VDD and GND respectively, which leads to the broadening of the hysteresis window. For the typical gate oxide materials, Fig. 4(b) shows that the switching voltage varies to VDD or GND slowly with the enhancement of the gate oxide dielectric permittivity. Besides, the switching voltage falls quickly and the hysteresis window narrows down with decreasing of the supply voltage, as shown in Fig. 4(c). This study helps circuit designers to choose the suitable device parameters when analyzing and designing the digital integrated circuits.

IV. CONCLUSIONS

In this work, we systematically explore the static characteristic of CMOS digital circuits using TMDs FETs and the influences of the device parameters on the performance of the CMOS combinational logic circuits. Through the circuit simulation, we find that the inverter with a gate oxide thickness of 2.8 nm and HfO_2 as the gate oxide material can obtain the best performance. An inverter with the same width of PMOS whose width is 64 nm and NMOS whose width is also 64 nm can obtain a large noise margin. Besides, a thinner gate oxide thickness of 2.8 nm can help broaden the hysteresis window of the Schmitt triggers obviously. The dielectric permittivity of gate oxide materials influences the output curve of the Schmitt triggers slightly. The lowest switching threshold of Schmitt triggers and the narrowest hysteresis window can be achieved when the supply voltage is 0.55 V. This work is meaningful for the Very Large Scale Integration (VLSI) circuit design and helps design special purpose CMOS circuit with unique features. The results can push ahead the design of logic circuits using TMDs FETs.

ACKNOWLEDGMENTS

This work was financially supported by the National Key R&D Program of China (grant nos. 2017YFA0303403 and 2018YFB0406500), the National Natural Science Foundation of China (grant nos. 61674057 and 91833303), Projects of Science and Technology Commission of Shanghai Municipality (grant nos. 18JC1412400, 18YF1407200, and 18YF1407000), and the Program for Professor of Special Appointment (Eastern Scholar) at Shanghai Institutions of Higher Learning.

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